

**AMENDMENTS TO THE CLAIMS**

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Claim 1. (Currently Amended) A frame-relay frame processing device for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell, wherein said device receives a frame-relay frame and writes said frame to a memory location shifted from a top of the next available memory location in a frame buffer.

Claim 2. (Currently Amended) A frame-relay frame processing device according to claim 1, wherein a size of the shift from the top of the next available memory location in the frame buffer is determined for each connection.

Claim 3. (Currently Amended) A frame relay circuit for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising:  
a processor for determining for each connection a size of a shift by which said frame is to be shifted from a top of the next available memory location in a frame buffer;  
a frame receiver for receiving said frame through said connection;  
a memory for storing said received frame at a location shifted from the top of the next available memory location in the frame buffer by said shift size; and  
a segmentation and reassembling device for reassembling said frame into said ATM cell.

Claim 4. (Previously Presented) A frame relay circuit according to claim 3, wherein, for each connection, said processor writes a data link connection

identifier (DLCI) and said shift size into a connection table, and retrieves said shift size from said connection table using said DLCI as a key.

Claim 5. (Previously Presented) A frame relay circuit according to claim 3, wherein said frame received by said frame receiver is transmitted to said memory through direct memory access.

Claim 6. (Currently Amended) A method for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising the steps of:

determining a shift size for each connection by which said frame is to be shifted from a top of the next available memory location in a frame buffer;

receiving said frame and writing said frame starting from an address shifted by said shift size; and

reassembling said frame into an ATM cell.

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Claim 7. (Previously Presented) A method according to claim 6, further comprising the steps of:

writing a data link connection identifier (DLCI) and said shift size into a connection table for each connection; and

retrieving said shift size from said connection table using said DLCI as a key.

Claim 8. (Previously Presented) A method according to claim 6, wherein said received frame is transmitted to said memory through direct memory access.

Claim 9. (Currently Amended) A computer readable medium containing program instructions for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell, the program instructions including instructions for performing the steps comprising:

determining a shift size for each connection by which said frame is to be shifted from a top address of the next available memory location in a frame buffer;

receiving said frame and writing said frame starting from an address shifted by said shift size; and

reassembling said frame into an ATM cell.

Claim 10. (Previously Presented) A computer readable medium according to claim 9, wherein said program instructions include instructions for:

writing a set of a data link connection identifier (DLCI) and said shift size into a connection table for each connection; and

retrieving said shift size in said connection table using said DLCI as a key.

Claim 11. (Original) A computer readable medium according to claim 9, wherein said received frame is transmitted to said memory through direct memory access.